

# Project overview

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# Introduction

- ◆ Photonics grows with an **Annual Growth Rate of 7.5%** and is considered a key enabling technology for the coming decades
- ◆ Europe has solid manufacturing base in photonics and specialty electronics.
- ◆ New opportunities in e.g. silicon photonics are increasingly commercialized in the US and the outsourced assembly and test industry is based in Asia.
- ◆ **Hybrid/heterogeneous integration will allow upscaling** of performance while allowing more complex applications. **Co-integration of ICs and PICs** is needed for further scaling.
- ◆ Main challenges: **miniaturization, scalability, temperature tolerance, solder reflow compatibility, packaging**. Need for **standardized and automated processes** e.g. fiber-chip, chip-chip alignment that can **drive down costs**.
- ◆ **Design for manufacturing, testability and packaging** to be considered from the very beginning to lead to commercialization

Source: Photonics21 Strategic Research and Innovation Agenda



# POLYNICES main driving ideas (I)

- ◆ Develop novel Electro-Optic PCB by spin-coating optical polymer on appropriate substrates
  - Provide low-cost “real-estate” for large scale PICs. Take advantage of PolyBoard toolbox.
  - Enable co-integration of electronic ICs for compact modules
- ◆ Develop TriPleX chiplets for different functionalities
  - Take advantage of TriPleX's high integration density. Develop multi-functional building blocks with standard interfaces that enable different kinds of photonic modules.
  - Standardization building blocks' interfaces to reduce assembly and packaging costs
- ◆ Develop processes for flip-chip integration the chiplets into the EOPCB. Establish wafer scale processes for electrical and optical interfacing
  - Take advantage of micro-electronics packaging concepts for dense electrical connections (e.g. “BGA like”) to alleviate the electrical IO bottleneck evident in large scale PICs e.g. QIPs
  - Use novel approaches like laser soldering to obviate the need for high-temp. solder-reflow that can disturb optical alignment



# POLYNICES main driving ideas (II)

- ◆ Optimize PZT actuators on TriPleX
  - Decrease PZT length for compactness. More elements per chiplet
  - Redesign PZTs with higher impedance to decrease power consumption
- ◆ Design and develop dielectric rod waveguides for THz frequencies
  - Antennas will improve Thz emitters' performance in beam steering e.g. compared to lenses.
- ◆ Define a process flow for the assembly of the demonstrators considering volume production
  - Combine all the EOPCB fabrication and assembly steps into a process flow
  - Standardize building blocks and interfaces, develop a Process Design Kit
- ◆ Develop compact and low-cost FMCW THz spectrometers and large mode QIPs to demonstrate POLYNICES technology
  - FMCW THz spectrometer versatile tool with numerous industrial applications but currently available mostly in high-cost bulk devices
  - Large mode QIPs suffer from electrical IO bottleneck
  - Applications driven by end users and aligned to their roadmaps with clear exploitation paths



# POLYNICES overview

## New generation of FMCW THz spectrometers and Quantum Information Processors based on novel photonic integration technology

### Vision - Concept

*"Development of a novel general purpose photonic integration technology, compatible with wafer scale processes that will reduce the production costs of photonic modules by 10x"*

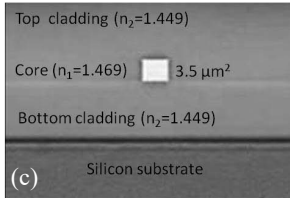
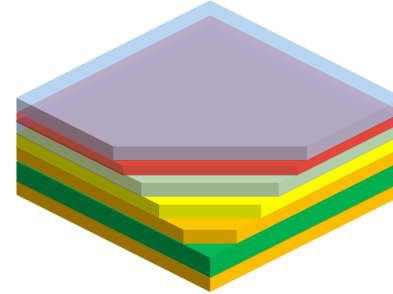
- ◆ Development of a novel **low-cost Electro-Optic PCB motherboard** based on optical polymers
- ◆ Development of novel **flip-chip compatible TriPleX chiplets and InP components** with different functionalities
- ◆ **Co-integration with electronic ICs** enabling compact photonic modules
- ◆ Development of **low-cost photonics-enabled FMCW THz spectrometers** with novel THz dielectric waveguide rod antennas focusing on industrial applications
- ◆ Development of **highly scalable Quantum Information Processors**, enabling large mode processors (24x24)



# POLYNICES objectives (I)

**Objective 1 | Select appropriate PCB substrate and develop a reliable process for spin-coating highly planar polymer surfaces and fabricating low-loss single mode waveguides**

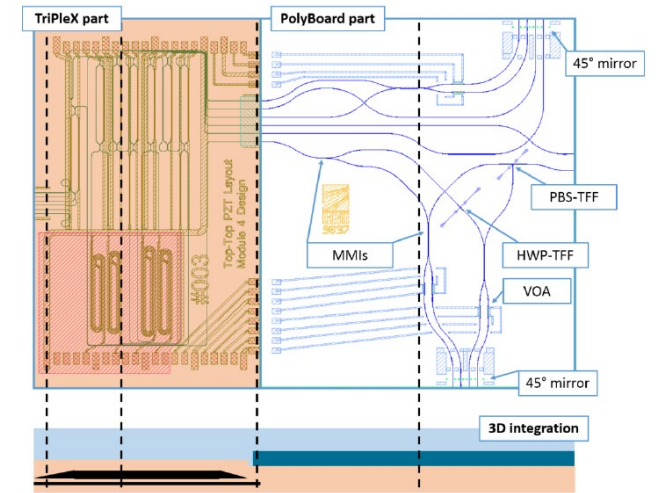
- Roughness: **< 1  $\mu\text{m}$**  deviation
- Waveguide propagation loss:  
**< 0.5 dB/cm** at 1550nm  
**< 0.2 dB/cm** at 780 nm
- Coupling loss to TriPleX chips: **< 0.2 dB/facet\***  
\*Spot-size converters



**Fraunhofer**  
Heinrich Hertz Institute

## Previous experience

- Spin-coating of polymer on TriPleX wafers with small etch depths for sensing applications (H2020 - 3PEAT project)



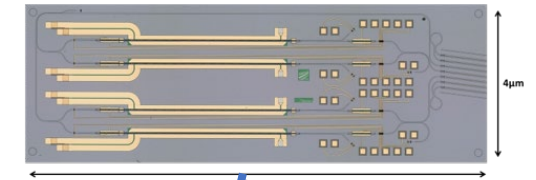
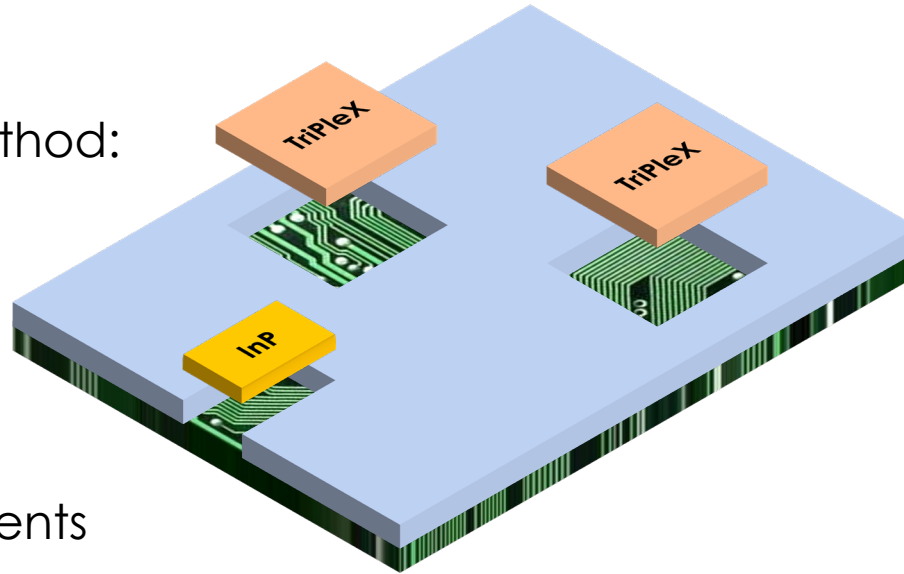
# POLYNICES objectives (II)

**Objective 2 | Develop the process for accurate etching of recesses in the motherboard that will enable flip-chip integration and passive alignment of photonic chiplets, micro-optic elements and InP elements**

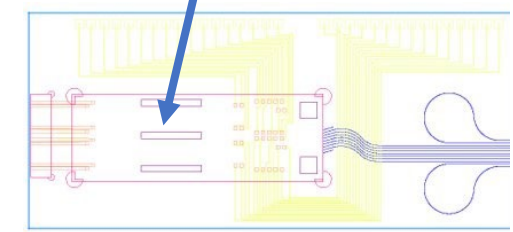
- Passive alignment stops
- Alignment accuracy of etching method: **< 500 nm**

## Previous experience

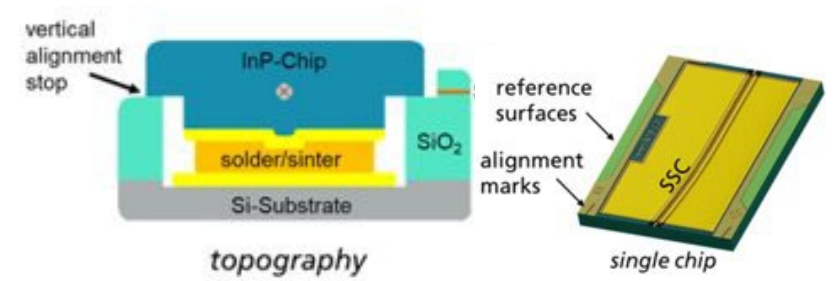
- Flip-chip integration of InP components on TriPleX and PolyBoard (H2020 – POETICS project)
- Integrated lenses and micro-optical elements for optical isolation (H2020 - 3PEAT project)



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InP modulator chip - PolyBoard



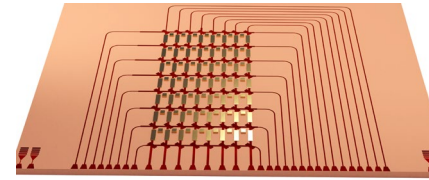
InP LD or PD chip - TriPleX



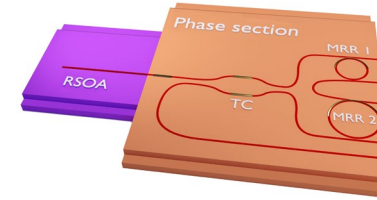
# POLYNICES objectives (III)

**Objective 3 | Develop multi-functional, flip-chip integration compatible Si3N4 PICs (chipslets), as photonic building blocks of highly scalable and low power consuming photonic integrated circuits**

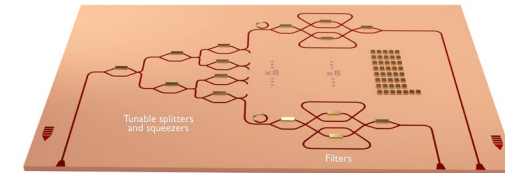
- 8x8 Blass matrix (BM-8)
- 8x8 Clements matrix (CM-8)
- Low linewidth ECL at 780 nm ECL (ECL-780)
- Low linewidth ECL at 1550 nm (ECL-1550)
- 1x8 squeezed light generator (SQ-8)
- Coupling loss: **< 0.2 dB/facet**  
using grating couplers and spot-size converters
- ECL Output power: **100 mW**



BM-8



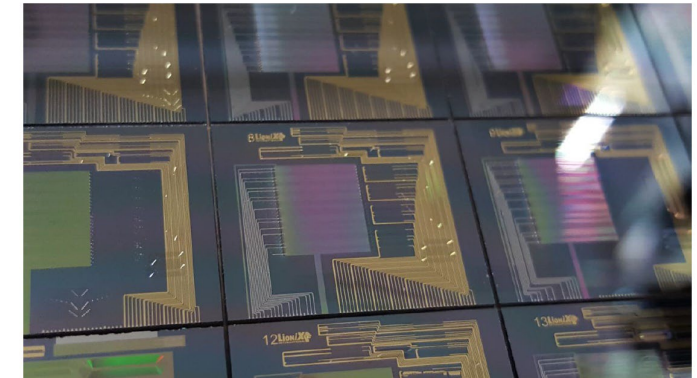
ECL 780,1550



SQ-8

## Previous experience

- Blass matrix PICs for beamforming (H2020 - HAMLET, H2020-TERAWAY)
- Low linewidth ECLs at 1550 nm for sensing and telecom (H2020 - 3PEAT, H2020-POETICS)
- LXI is designing QIP PICs for QUIX products



H2020 - HAMLET

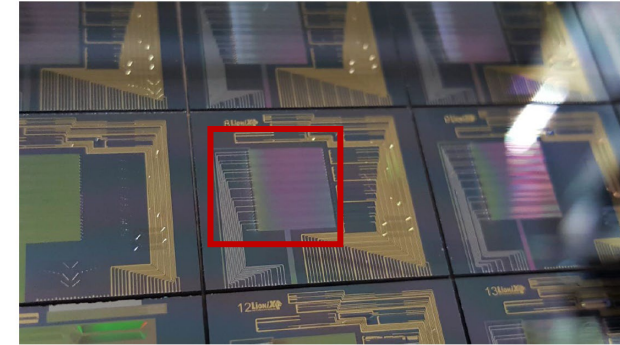
# POLYNICES objectives (IV)

## Objective 4 | Develop of compact, high speed and low driving voltage PZT stress optic actuators

- Speed: > **10 MHz**
- Driving voltage 2pi : < **40 V**
- PZT length : **5 mm**

### Previous experience

- PZT elements on TriPleX PICs (~1.5 cm long) (H2020 – HAMLET, H2020 – 3PEAT)



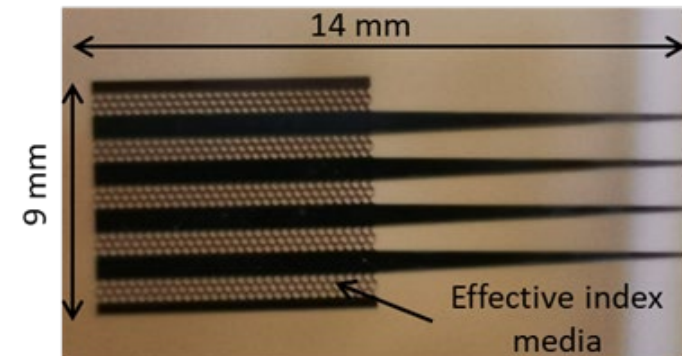
**LioniX**  
INTERNATIONAL

## Objective 5 | Develop single and arrayed versions of THz antennas with dielectric rods for high gain over a wide dynamic frequency range and low crosstalk

- Frequency range: > **1 THz**
- Gain : > **20 dBi**
- Crosstalk : < **-20 dB**
- Pitch : < **1 mm**

### Previous experience

- Rod waveguides for THz communications (H2020-TERAWAY)



**uc3m**  
Universidad  
Carlos III  
de Madrid



# POLYNICES objectives (V)

## Objective 6 | Develop a wafer scale process for low-loss flip-chip integration and investigate laser soldering of Si<sub>3</sub>N<sub>4</sub> chipllets into the EOPCB motherboard

- Coupling loss: < **0.2 dB/facet**  
using grating couplers and spot size converters
- Pick and place time incl. soldering : < **1.5 min /chipllet**

### Previous experience

- Assembly automation of PICs for optical transceivers targeting volume production (H2020 – TERIPHIC, H2020 – POETICS)

## Objective 7 | Develop process for co-packaging of the electronic ICs with the motherboard, combine individual steps and consolidate a single process flow for the assembly and packaging of POLYNICES demonstrators

- Define process flow steps
- Assess the compatibility of the processes (e.g soldering order of ICs and chipllets)
- Consolidate them into a single process flow

### Previous experience

- Co-packaging of optical engines with ASICs. Process flow definition for volume production (H2020 – POETICS, H2020 – TERIPHIC)



# POLYNICES objectives (VI)

## **Objective 8 | Develop the demonstrators of POLYNICES technology for FMCW THz spectrometer and QIP**

- 2 FMCW demonstrators (Demo 1A, Demo 1B)
- 2 QIP demonstrators (Demo 2A, Demo 2B)

## **Objective 9 | System evaluation of POLYNICES demonstrators and validation of their performance in relevant settings**

- Component level tests
- System tests at laboratory
- System tests at vendor

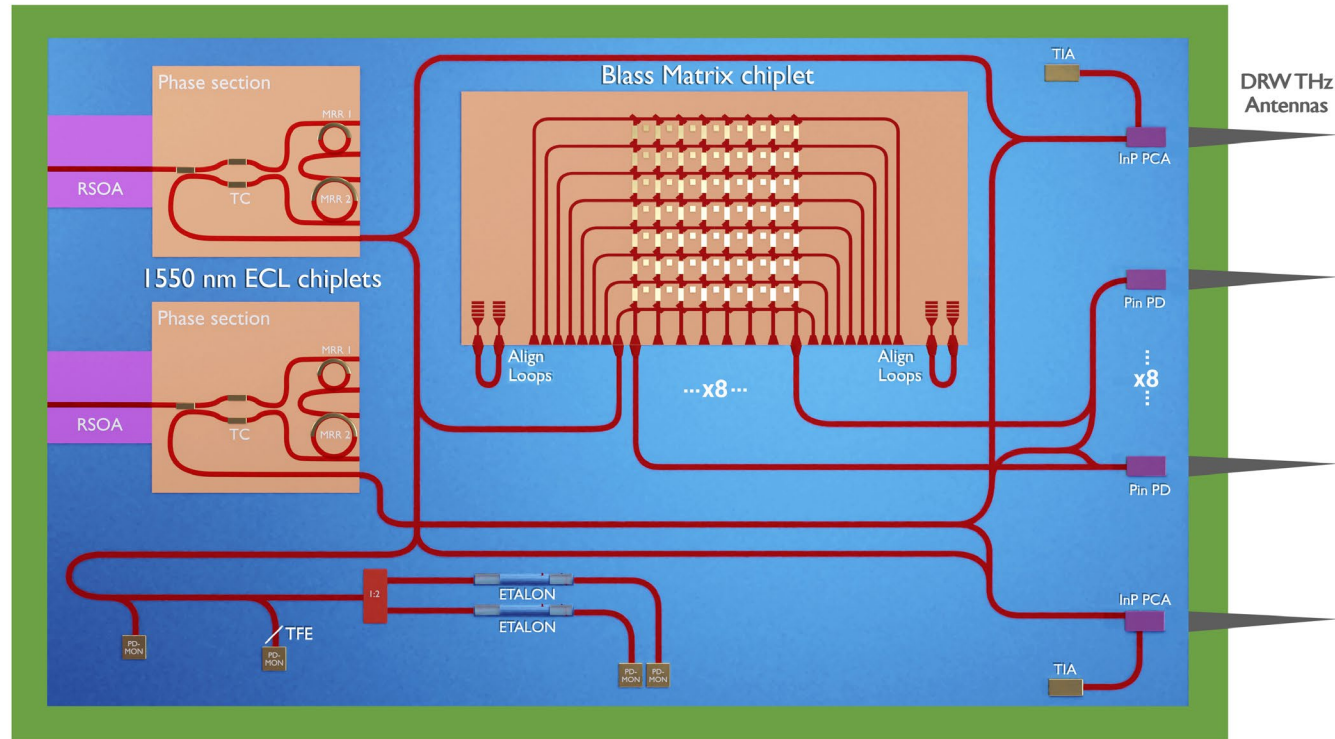
## **Objective 10 | Consolidation of a commercialization strategy and definition of a Process Design Kit (PDK) that will lower the barrier for stakeholders to use POLYNICES technology**

- Define PDK with building blocks
- Effort to standardize packaging
- Offer POLYNICES technology through Multi-Project Wafer (MPW) runs to customers



# POLYNICES demonstrators

## FMCW THz spectrometer with beam-steering functionality (Demo-1B)

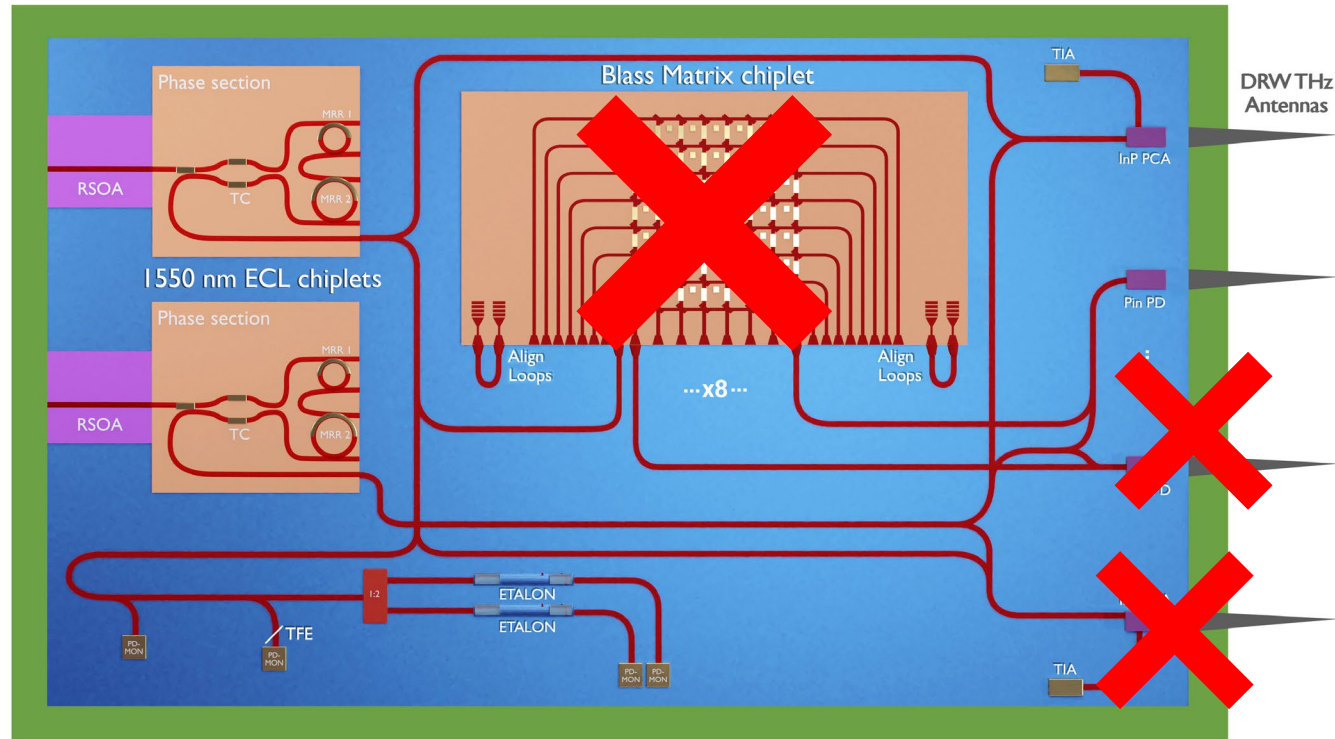


- EOPCB motherboard
  - 2x ECL-1550
  - 1x BM-8
  - 8x Pin PDs
  - 10x Dielectric rod antennas
  - 2x InP PhotoCond. Antennas
  - 2x TIAs
  - Wavelength meter
- Specs to be defined in T2.1 (e.g. field of view, RF output power etc)



# POLYNICES demonstrators

## FMCW THz spectrometer precursor (Demo-1A)

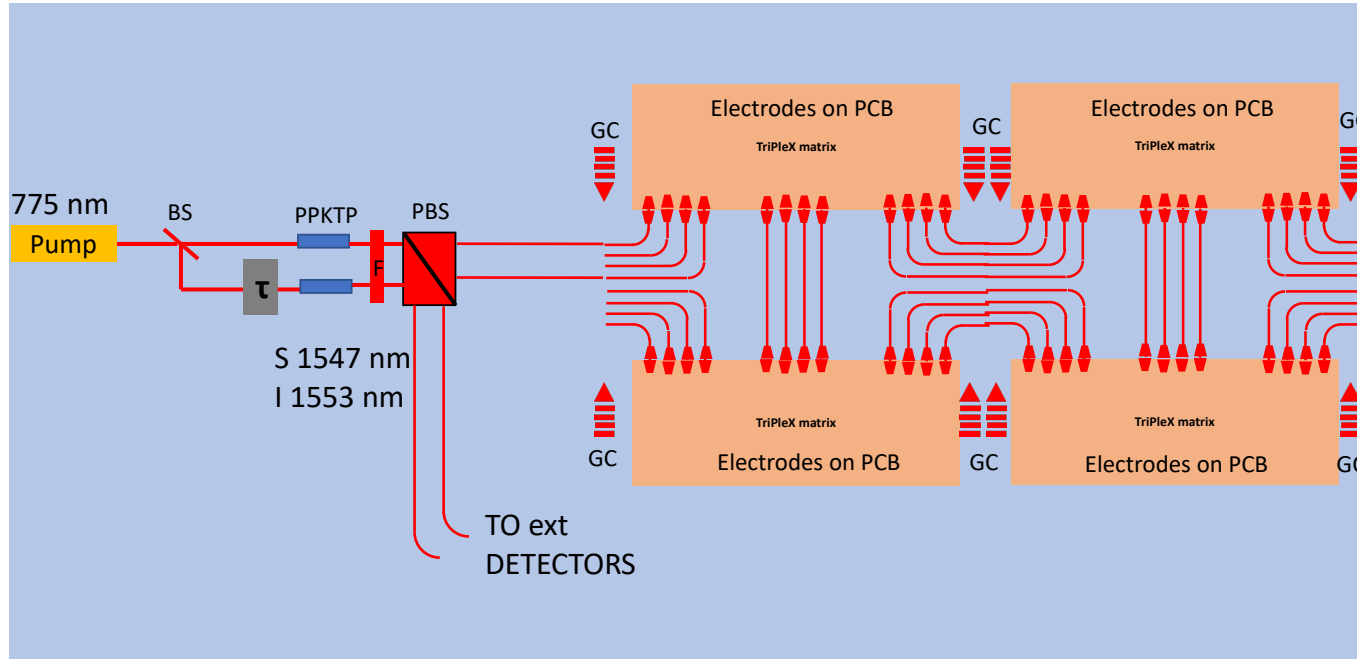


- EOPCB motherboard
  - 2x ECL-1550
  - 1x Pin PDs
  - 2x Dielectric rod antennas
  - 1x InP PhotoCond. Antennas
  - 1x TIA
  - Wavelength meter
- Specs to be defined in T2.1

- Demo-1A will not have beam-steering functionality

# POLYNICES demonstrators

## 16x16 QIP with integrated 780 nm pump and non-linear crystals (Demo-2A)



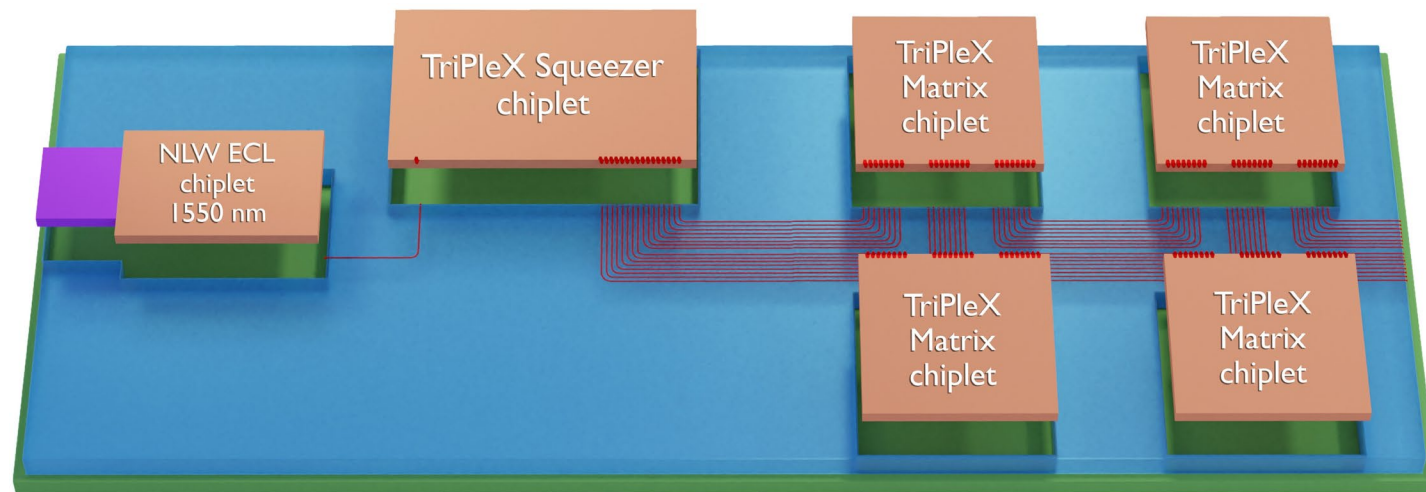
- EOPCB motherboard
  - 4x CM-8
  - 1x ECL-780
  - PPKTP crystals
  - Optical filter

- External detectors

- Specs to be defined in T2.1

# POLYNICES demonstrators

## 24x24 QIP with integrated 1550 nm pump and squeezed light generator (Demo-2A)

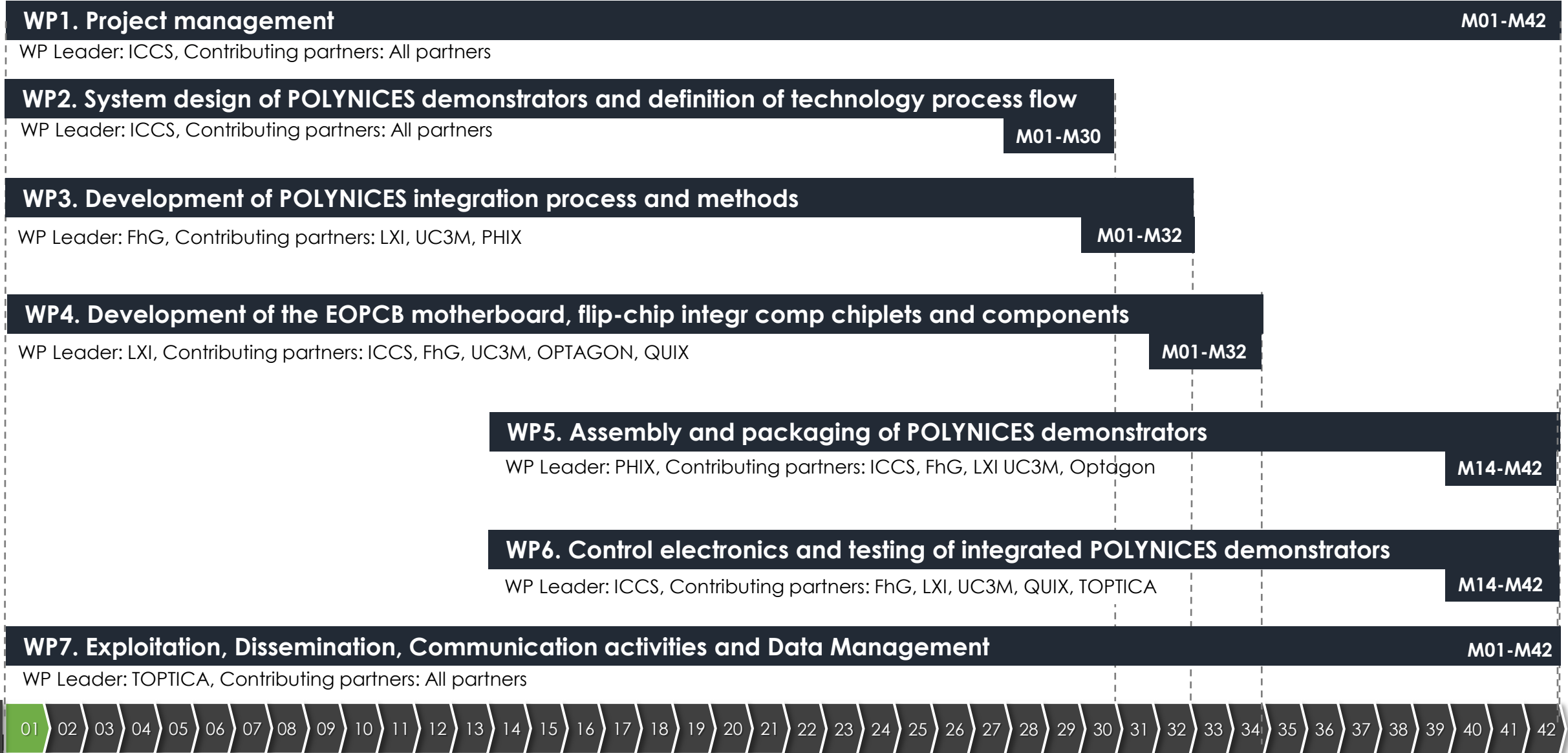


- EOPCB motherboard
  - 1x ECL-1550
  - 1x SQ-8
  - 9x CM-8
- External detectors
- Specs to be defined in T2.1

- Example schematic showing only 4 matrix chiplets



# Work Packages - Timeline



Project Month



# WP2. System design of POLYNICES demonstrators and definition of technology process flow

WP2 Leader: ICCS, Contributing partners: All partners

Duration: M01 – M30 | PMs: 69

**T2.1** – System design of POLYNICES demonstrators and definition of technology process flow [M01-M24]



**T2.2** – Design of process flow, integration methods and packaging approach [M01-M24]



**T2.3** – Design of single and arrayed THz antennas [M01-M30]



**T2.4** - Assembly and packaging process: design and specifications [M01-M30]



# WP3. Development of POLYNICES integration process and methods

WP3 Leader: FhG-HH, Contributing partners: LXI, UC3M, PHIX

Duration: M01 – M32 | PMs: 74

**T3.1** – Heterogeneous integration of polymer layers on the PCB substrate [M01-M32]



**T3.2** – Development of etching processes and micro-optic bench [M01-M32]



**T3.3** – Development of flip-chip integration process for the chipelets and InP elements [M01-M32]



**T3.4** – Development of PZT phase actuators on TriPleX chipelets [M01-M32]



**T3.5** – Development of soldering process for the integration of PICs and ICs [M01-M32]



# WP4. Development of the EOPCB motherboard, flip-chip integration compatible chiplets and components

**WP4 Leader: LXI, Contributing partners: FhG-HHI, UC3M, Optagon, QUIX**  
**Duration: M01 – M32 | PMs: 84**

**T4.1** – Development of EOPCB motherboards for the demonstrators [M01-M32]



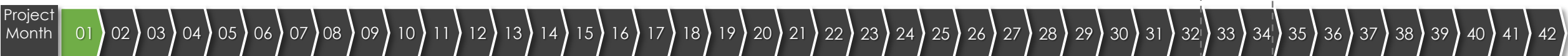
**T4.2** – Development of Quantum Photonics Processor Clements Matrix, Blass Matrix and Squeezer chiplets [M01-M32]



**T4.3** – Development of 780 nm and 1550 nm External Cavity Laser chiplets [M01-M32]



**T4.4** – Development of InP THz emitters and receivers [M01-M34]



# WP5. Assembly and packaging of POLYNICES demonstrators

WP5 Leader: PHIX, Contributing partners: ICCS, FhG-HHI, LXI, UC3M, Optagon, QUIX

Duration: M14 – M42 | PMs: 58



**T5.1** – Development of the packaging engine [M14-M24]



**T5.2** – Electronic design of the EOPCB [M14-M42]



**T5.3** – Assembly and packaging of FMCW THz spectr. demonstrators [M19-M42]



**T5.4** – Development of InP THz emitters and receivers [M19-M42]



# WP6. Control electronics and testing of integrated POLYNICES demonstrators

WP6 Leader: ICCS, Contributing partners: FhG-HHI, LXI, UC3M, Optagon, QUIX

Duration: M14 – M42 | PMs: 61



**T6.1** – Definition of testing methodology, setting up system testbeds [M14-M26]



**T6.2** – Development of driving and read-out electronics for POLYNICES demonstrators [M14-M42]



**T6.3** – System integration and testing of FMCW THz spectrometer demonstrators [M19-M42]



**T6.4** – System integration and testing of QIP demonstrators [M19-M42]



# WP7. Exploitation, Dissemination, Communication activities and Data Management

**WP7 Leader: TOPTICA, Contributing partners: All partners**  
**Duration: M01– M42 | PMs: 40**

**T7.1** – Market analysis and roadmapping [M01-M42]



**T7.2** – Exploitation of foreground knowledge and business planning [M01-M42]



**T7.3** – Protection, management of IPR and Data Management [M01-M42]



**T7.4** – Dissemination, communication and clustering activities [M01-M42]

